



HGK70R240E-W

700V GaN Enhancement-mode Power Transistor

1. General description

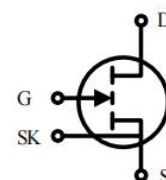
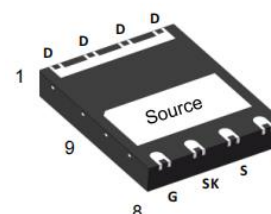
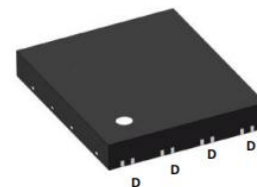
700V GaN-on-Silicon Enhancement-mode Power Transistor in package DFN5*6

2. Features

- Enhancement mode transistor-Normally off power switch
- Ultra high switching frequency
- No reverse-recovery charge
- Low gate charge, low output charge
- Qualified for industrial applications according to JEDEC Standards
- ESD safeguard
- RoHS, Pb-free, REACH-compliant

3. Applications

- AC-DC converters
- DC-DC converters
- Totem pole PFC
- Fast battery charging
- High density power conversion
- High efficiency power conversion



4. Key performance parameters

Table 1 Key performance parameters at $T_j = 25\text{ }^{\circ}\text{C}$

Parameter	Value	Unit
$V_{DS,max}$	700	V
$R_{DS(on),max} @ V_{GS} = 6V$	240	$m\Omega$
$Q_{G,typ} @ V_{DS} = 400V$	2	nC
$I_{D,pulse}$	18	A
$Q_{OSS} @ V_{DS} = 400V$	21	nC
$Q_{rr} @ V_{DS} = 400V$	0	nC

5. Pin information

Table 2 Pin information

Gate	Drain	Kelvin Source	Source
8	1,2,3,4	7	5,6,9

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
HGK70R240E-W	DFN5*6	HGK70R240E-W



HGK70R240E-W

700V GaN Enhancement-mode Power Transistor

6. Maximum ratings

at $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Exceeding the maximum ratings may destroy the device. For further information, contact Huake sales office.

Table 4 Maximum ratings

Parameter	Symbol	Values	Unit	Note/Test Condition
Drain source voltage	$V_{DS,max}$	700	V	$V_{GS} = 0\text{ V}$, $T_j = -55\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$
Drain source voltage transient ¹	$V_{DS(transient)}$	800	V	$V_{GS} = 0\text{ V}$
Drain source voltage, pulsed ²	$V_{DS,pulse}$	750	V	$T_j = 25\text{ }^{\circ}\text{C}$; total time < 10h
Drain source voltage, pulsed ²	$V_{DS,pulse}$	750	V	$T_j = 125\text{ }^{\circ}\text{C}$; total time < 1h
Continuous current, drain source	I_D	10	A	$T_c = 25\text{ }^{\circ}\text{C}$
Pulsed current, drain source ³	$I_{D,pulse}$	18	A	$T_c = 25\text{ }^{\circ}\text{C}$; $V_G = 6\text{ V}$; $t_{PULSE} = 10\mu\text{s}$
Pulsed current, drain source ³	$I_{D,pulse}$	10	A	$T_c = 125\text{ }^{\circ}\text{C}$; $V_G = 6\text{ V}$; $t_{PULSE} = 10\mu\text{s}$
Gate source voltage, continuous ⁴	V_{GS}	-1.4 to +7	V	$T_j = -55\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$
Gate source voltage, pulsed	$V_{GS,pulse}$	-20 to +10	V	$T_j = -55\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$; $t_{Pulse} = 50\text{ ns}$, $f = 100\text{ kHz}$ open drain
Power dissipation	P_{tot}	73	W	$T_c = 25\text{ }^{\circ}\text{C}$
Operating temperature	T_j	-55 to +150	$^{\circ}\text{C}$	
Storage temperature	T_{stg}	-55 to +150	$^{\circ}\text{C}$	

1 $V_{DS(transient)}$ is intended for non-repetitive events, $t_{PULSE} < 200\text{ }\mu\text{s}$

2 $V_{DS,pulse}$ is intended for repetitive pulse, $t_{PULSE} < 100\text{ ns}$

3 Limit was extracted from characterization test, not measured during production

4 The minimum V_{GS} is clamped by ESD protection circuit, as shown in Figure 10

7. Thermal characteristics

Table 5 Thermal characteristics

Parameter	Symbol	Values	Unit	Note/Test Condition
Thermal resistance, junction-case	R_{thJC}	1.71	$^{\circ}\text{C/W}$	
Maximum reflow soldering temperature	T_{sold}	260	$^{\circ}\text{C}$	MSL3



HGK70R240E-W

700V GaN Enhancement-mode Power Transistor

8. Electric characteristics

at $T_j = 25\text{ }^{\circ}\text{C}$, unless specified otherwise

Table 6 Static characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	1.2	1.7	2.5	V	$I_D=11\text{mA}$; $V_{DS}=V_{GS}$; $T_j=25\text{ }^{\circ}\text{C}$
		--	1.7	--		$I_D=11\text{mA}$; $V_{DS}=V_{GS}$; $T_j=150\text{ }^{\circ}\text{C}$
Drain-source leakage current	I_{DSS}	--	0.4	20	μA	$V_{DS}=700\text{V}$; $V_{GS}=0\text{V}$; $T_j=25\text{ }^{\circ}\text{C}$
		--	5	--		$V_{DS}=700\text{V}$; $V_{GS}=0\text{V}$; $T_j=150\text{ }^{\circ}\text{C}$
Gate-source leakage current	I_{GSS}	--	50	--	μA	$V_{GS}=6\text{V}$; $V_{DS}=0\text{V}$
Drain-source on-state resistance	$R_{DS(on)}$	--	165	240	$\text{m}\Omega$	$V_{GS}=6\text{V}$; $I_D=3\text{A}$; $T_j=25\text{ }^{\circ}\text{C}$
		--	360	--		$V_{GS}=6\text{V}$; $I_D=3\text{A}$; $T_j=150\text{ }^{\circ}\text{C}$
Gate resistance	R_G	--	6	--	Ω	$f=5\text{MHz}$; open drain

Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	--	79	--	pF	$V_{GS}=0\text{V}$; $V_{DS}=400\text{V}$; $f=100\text{kHz}$
Output capacitance	C_{oss}	--	25	--	pF	$V_{GS}=0\text{V}$; $V_{DS}=400\text{V}$; $f=100\text{kHz}$
Reverse transfer capacitance	C_{rss}	--	0.2	--	pF	$V_{GS}=0\text{V}$; $V_{DS}=400\text{V}$; $f=100\text{kHz}$
Effective output capacitance, energy related ¹	$C_{o(er)}$	--	36	--	pF	$V_{GS}=0\text{V}$; $V_{DS}=0\text{ to }400\text{V}$
Effective output capacitance, time related ²	$C_{o(tr)}$	--	52	--	pF	$V_{GS}=0\text{V}$; $V_{DS}=0\text{ to }400\text{V}$
Output charge	Q_{OSS}	--	21	--	nC	$V_{GS}=0\text{V}$; $V_{DS}=0\text{ to }400\text{V}$
Turn-on delay time	$t_{d(on)}$	--	2	--	ns	$V_{DS}=400\text{V}$; $I_D=6\text{A}$; $L=318\text{ }\mu\text{H}$; $V_{GS}=6\text{V}$; $R_{on}=10\text{ }\Omega$; $R_{off}=2\text{ }\Omega$; See Figure 22
Turn-off delay time	$t_{d(off)}$	--	4	--	ns	
Rise time	t_r	--	5	--	ns	
Fall time	t_f	--	6	--	ns	

1 $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V

2 $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V

	HGK70R240E-W
	700V GaN Enhancement-mode Power Transistor

Table 8 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate charge	Q_G	--	2	--	nC	$V_{GS} = 0 \text{ to } 6 \text{ V}; V_{DS} = 400 \text{ V}; I_D = 3 \text{ A}$
Gate-source charge	Q_{GS}	--	0.2	--	nC	
Gate-drain charge	Q_{GD}	--	0.7	--	nC	
Gate Plateau Voltage	V_{Plat}	--	2.5	--	V	$V_{DS} = 400 \text{ V}; I_D = 3 \text{ A}$

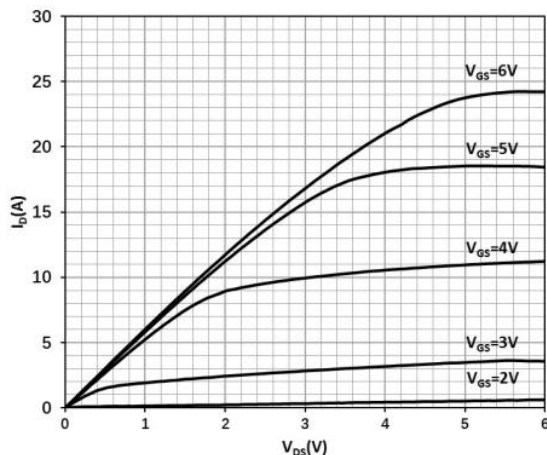
Table 9 Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}	--	2.6	--	V	$V_{GS} = 0 \text{ V}; I_{SD} = 3 \text{ A}$
Pulsed current, reverse	$I_{S,pulse}$	--	--	18	A	$V_{GS} = 6 \text{ V}; t_{PULSE} = 10 \mu s$
Reverse recovery charge	Q_{rr}	--	0	--	nC	$I_{SD} = 3 \text{ A}; V_{DS} = 400 \text{ V}$
Reverse recovery time	t_{rr}	--	0	--	ns	
Peak reverse recovery current	I_{rrm}	--	0	--	A	

9. Electric characteristics diagrams

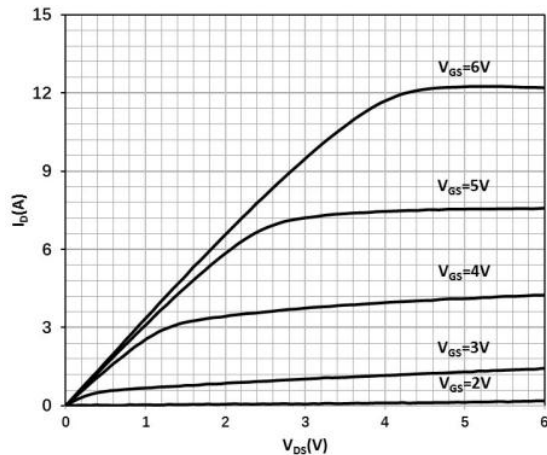
at $T_j = 25^\circ\text{C}$, unless specified otherwise

Figure 1 Typ. output characteristics



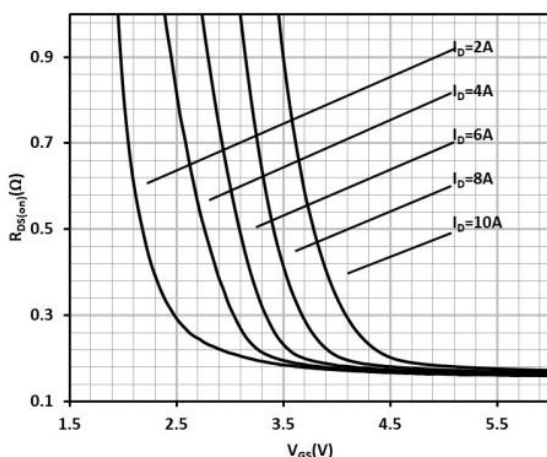
$$I_D = f(V_{DS}, V_{GS}); T_j = 25^\circ\text{C}$$

Figure 2 Typ. output characteristics



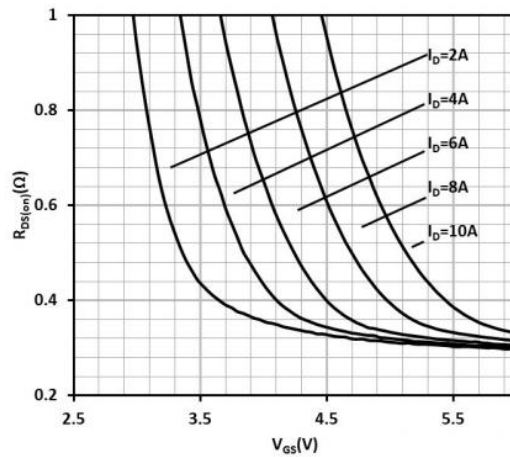
$$I_D = f(V_{DS}, V_{GS}); T_j = 125^\circ\text{C}$$

Figure 3 Typ. Drain-source on-state resistance



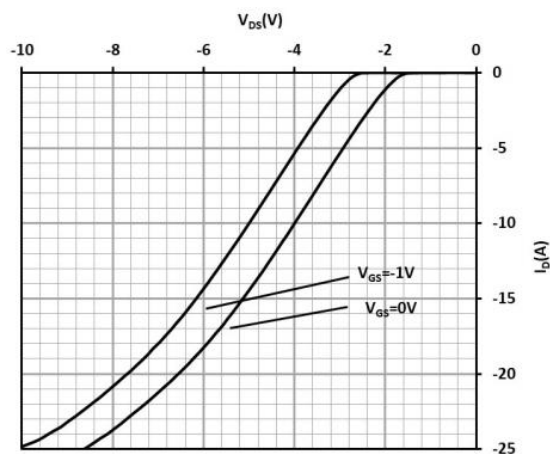
$$R_{DS(on)} = f(I_D, V_{GS}); T_j = 25^\circ\text{C}$$

Figure 4 Typ. Drain-source on-state resistance



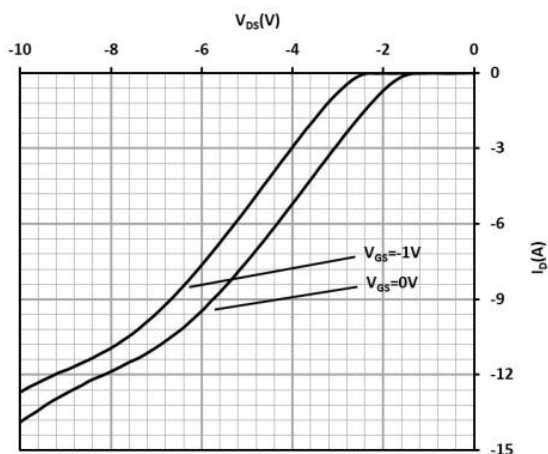
$$R_{DS(on)} = f(I_D, V_{GS}); T_j = 125^\circ\text{C}$$

Figure 5 Typ. channel reverse characteristics



$$I_D = f(V_{DS}, V_{GS}); T_j = 25^\circ\text{C}$$

Figure 6 Typ. channel reverse characteristics



$$I_D = f(V_{DS}, V_{GS}); T_j = 125^\circ\text{C}$$

Figure 7 Typ. channel reverse characteristics

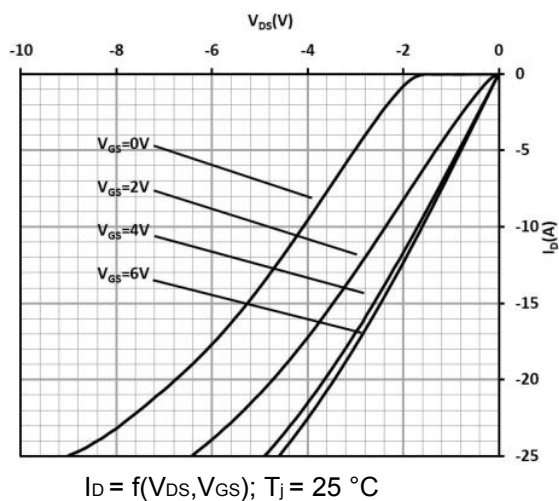


Figure 8 Typ. channel reverse characteristics

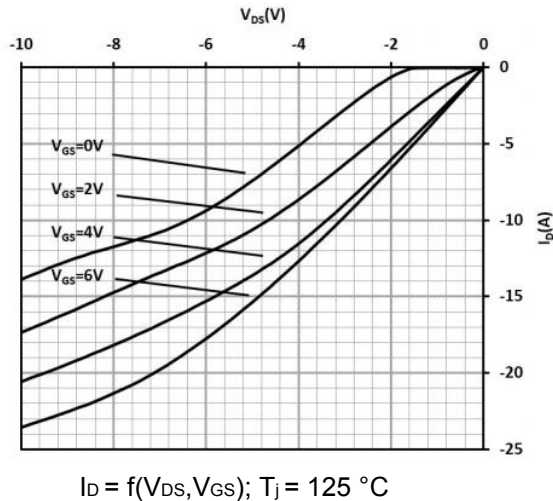


Figure 9 Typ. transfer characteristics

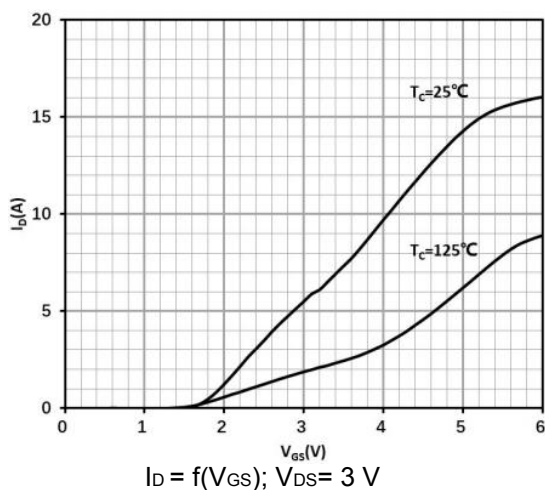


Figure 10 Typ. Gate-to-Source leakage

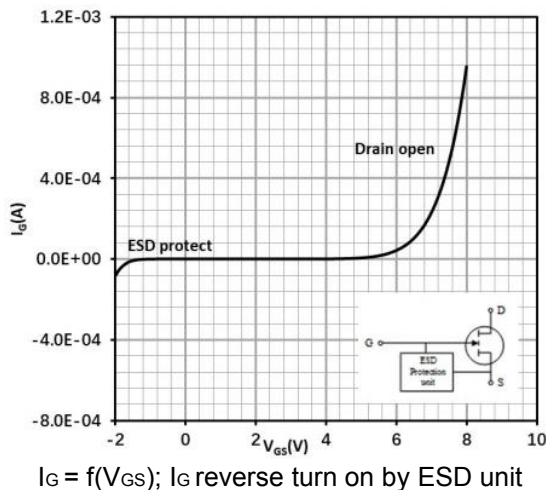


Figure 11 Drain-source leakage characteristics

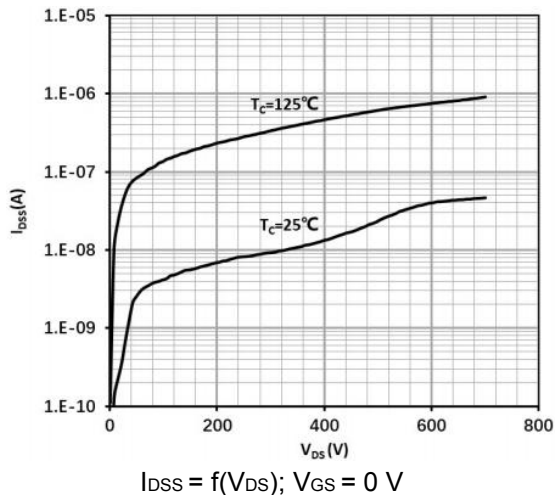
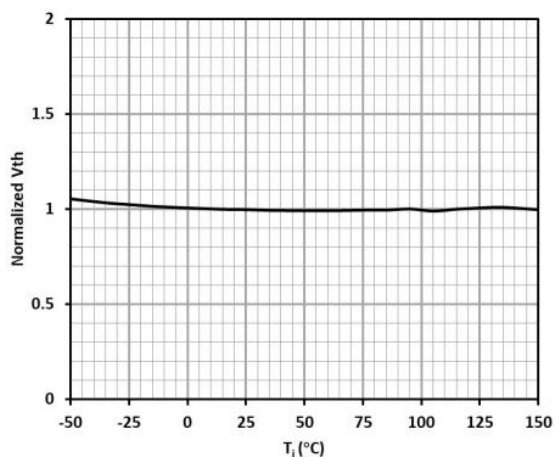
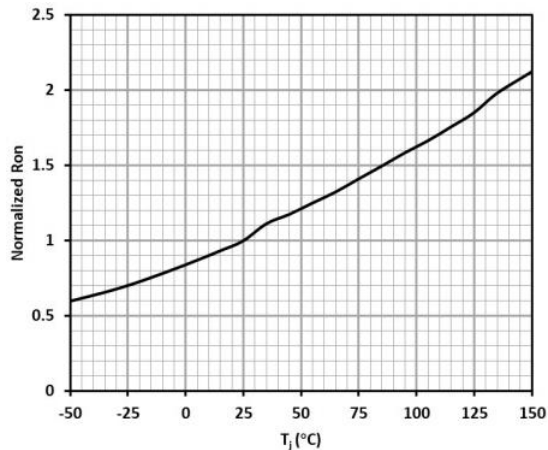


Figure 12 Gate threshold voltage



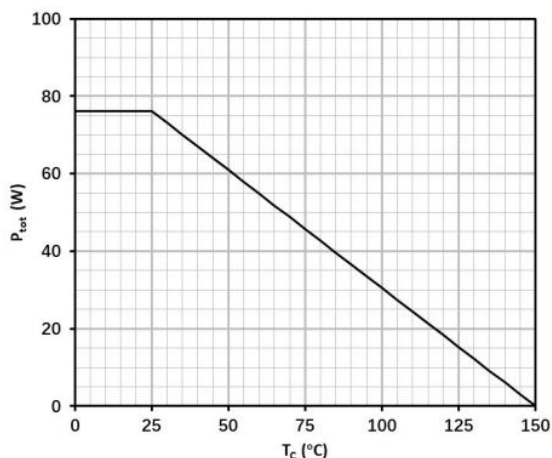
$$V_{TH} = f(T_j); V_{GS} = V_{DS}; I_D = 11 \text{ mA}$$

Figure 13 Drain-source on-state resistance



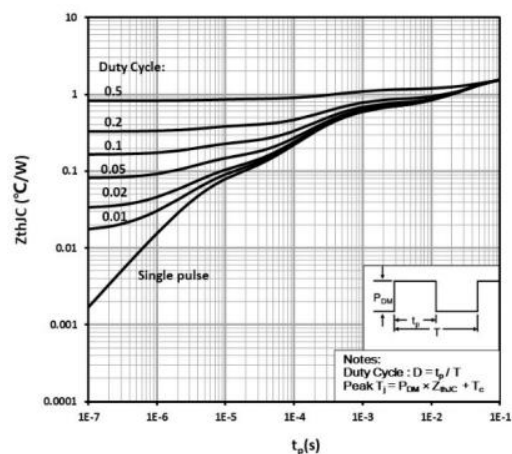
$$R_{DS(on)} = f(T_j); I_D = 3 \text{ A}; V_G = 6 \text{ V}$$

Figure 14 Power dissipation



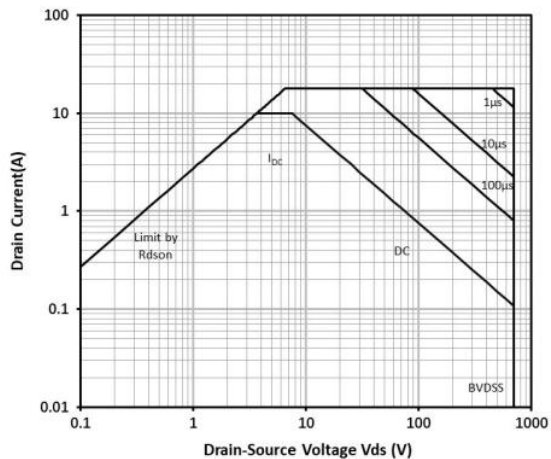
$$P_{tot} = f(T_c)$$

Figure 15 Max. transient thermal impedance



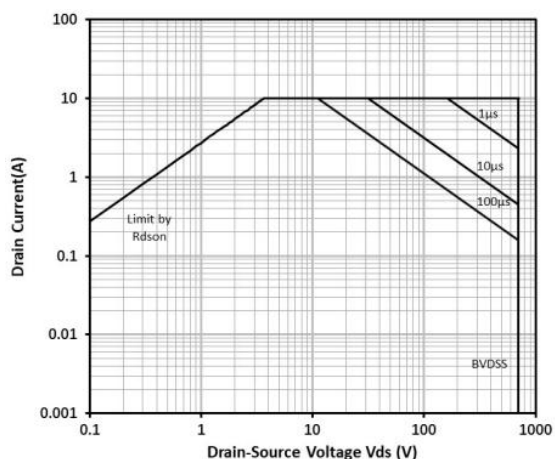
$$Z_{thJC} = f(t_p, D)$$

Figure 16 Safe operating area



$$I_D = f(V_{DS}); T_C = 25^\circ \text{C}$$

Figure 17 Safe operating area



$$I_D = f(V_{DS}); T_C = 125^\circ \text{C}$$

Figure 18 Typ. gate charge

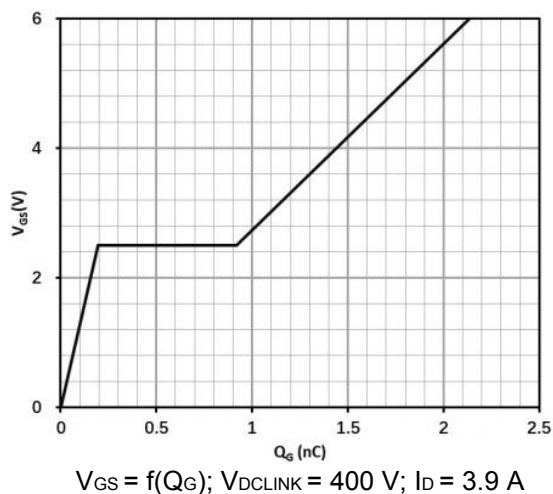


Figure 19 Typ. capacitances

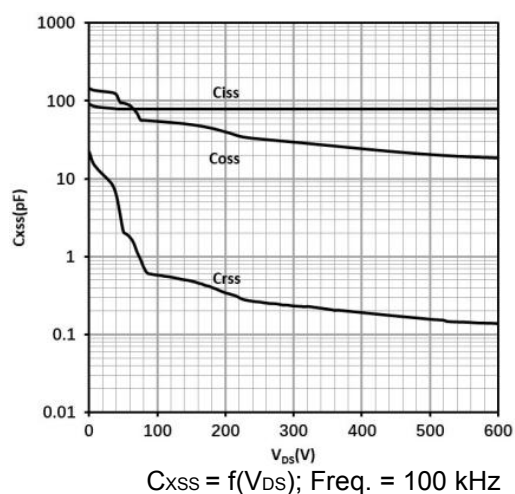


Figure 20 Typ. output charge

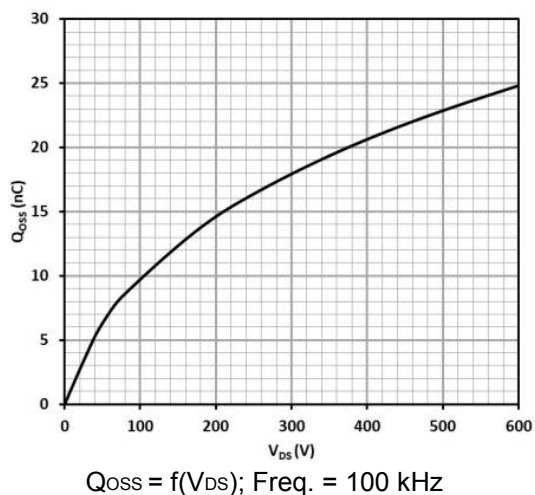


Figure 21 Typ. Coss stored Energy

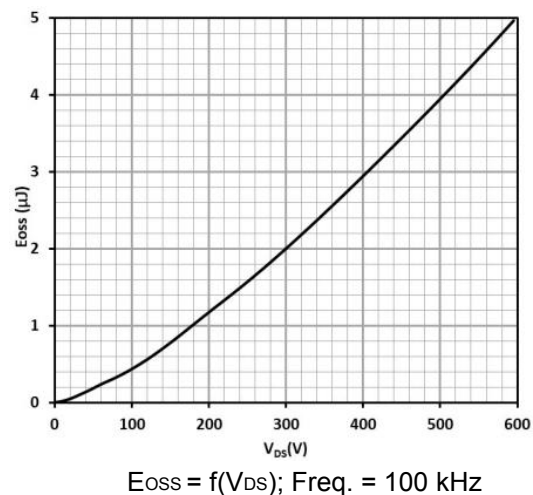
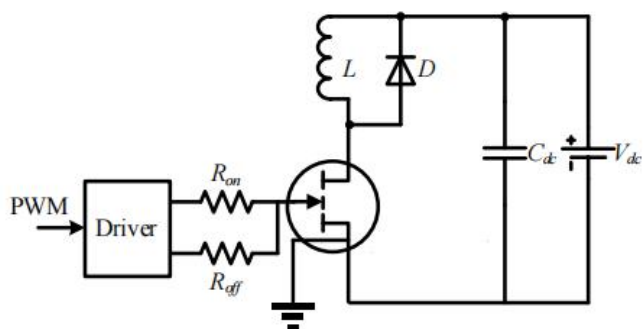
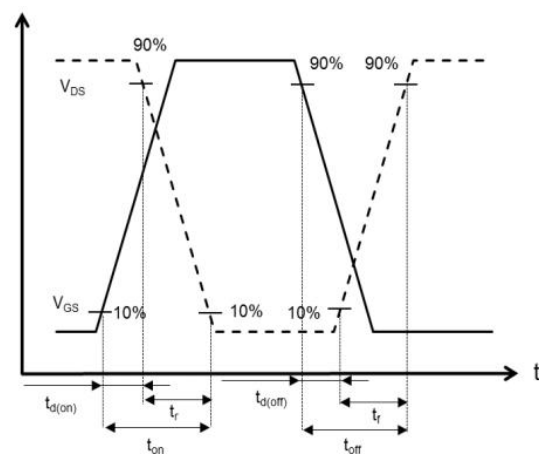


Figure 22 Typ. Switching times with inductive load



$V_{DS}=400\text{V}, I_D=6\text{A}, L=318\mu\text{H}, V_{GS}=6\text{V},$
 $R_{on}=10\Omega, R_{off}=2\Omega$

Figure 23 Typ. Switching times waveform

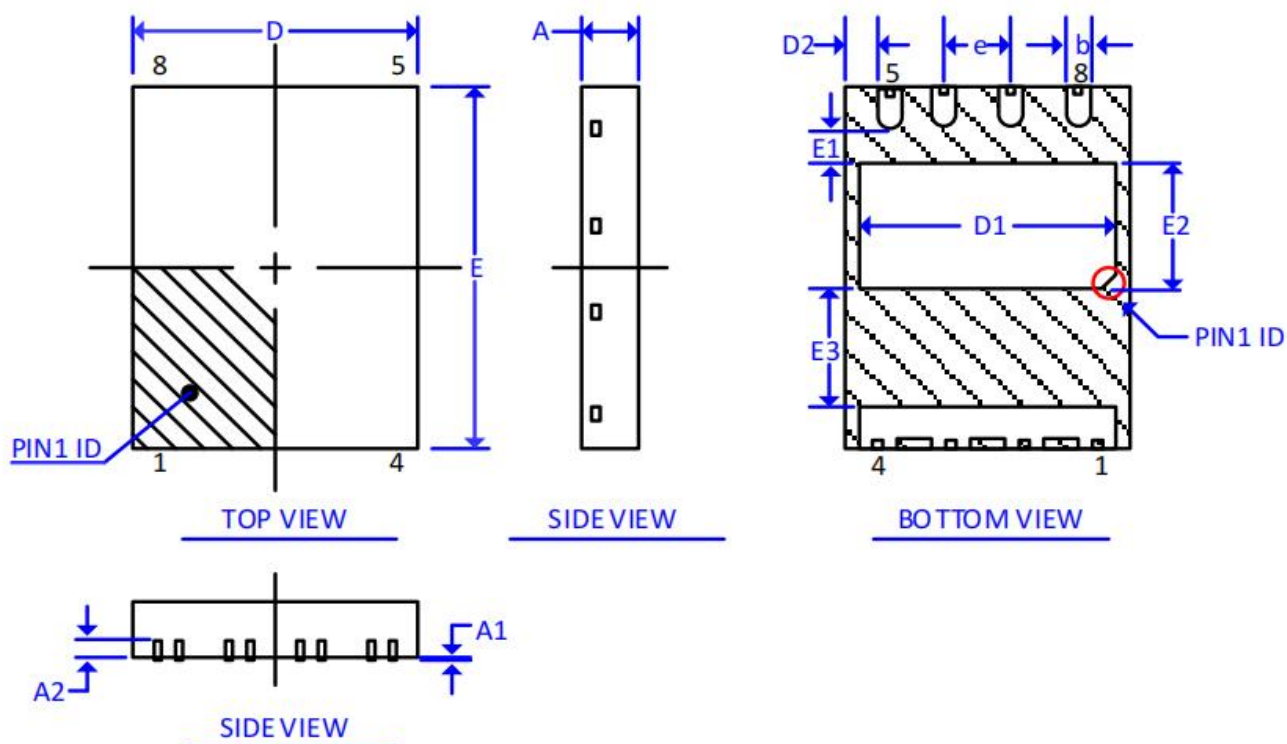


10.Package outlines

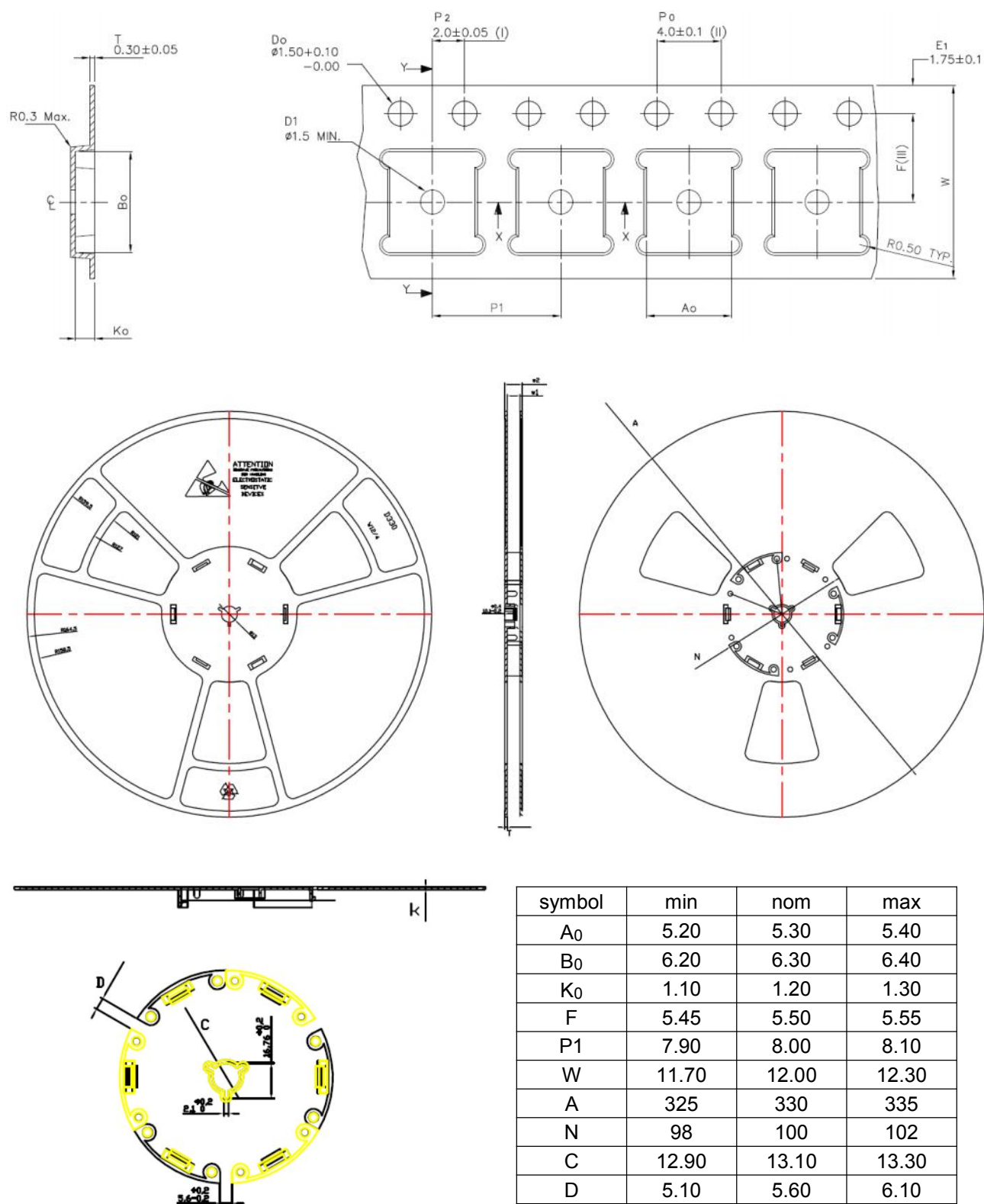
DFN5*6-8L Package Dimensions

UNIT: mm

symbol	min	nom	max	symbol	min	nom	max
A	0.80	0.90	1.00	E	6.00B.S.C		
A1	0.00	0.02	0.05	E1	0.40	0.50	0.60
A2	--	0.203ref	--	E2	1.95	2.05	2.15
b	0.40	0.45	0.50	E3	--	2.10	--
D	5.00B.S.C			e	1.27B.S.C		
D1	4.16	4.26	4.36	L	0.575	0.675	0.775
D2	0.27	0.37	0.47				



11.Reel Information



	HGK70R240E-W
	700V GaN Enhancement-mode Power Transistor

Important Notice

The information provided in this document is intended as a guide only and shall not in any event be regarded as a guarantee of conditions, characteristics or performance. Huake does not assume any liability arising out of the application or use of any product described herein, including but not limited to any personal injury, death, or property or environmental damage. No licenses, patent rights, or any other intellectual property rights is granted or conveyed. Huake reserves the right to modify without notice. All rights reserved.

版本履历表:

序号	版本号	修改时间	修改记录
1	V1.0	2023-3-21	首次发行